DECLARATION

I, the below-named translator, hereby declare:

(1) That my name, mailing address and citizenship are as stated below;

(2) That I am knowledgeable in the English language and in the Korean language in which Korean Patent Application No. 03-11767 was filed on February 25, 2003; and

(3) That I have translated said Korean Patent Application No. 03-11767 into English, whose English text is attached hereto, and believe that said translation is a true and complete translation of the aforementioned Korean patent application.

July 3, 2007

Full name of the translator: Kyung Gu Kang

Signature of the translator: _____

Mailing address: Kamryoung Building, 3rd Floor, 153-29, Samsung-dong, Kangnam-ku, Seoul, Republic of Korea

STATUTORY DECLARATION

I, Kyung Gu KANG, a citizen of the Republic of Korea and a staff member of Y.H.KIM INTERNATIONAL PATENT & LAW OFFICE specializing in "METHOD AND APPARATUS FOR DRIVING PLASMA DISPLAY PANEL" do hereby declare that:

I am conversant with the English and Korean languages and a competent translator thereof.

To the best of my knowledge and belief, the following is a true and correct translation of the Relativity Document (No. P2003-11767) in the Korean language already filed with Korean Industrial Property Office on February 25, 2003.

Signed this 3rd day of June, 2007

Kyung Gu KANG

PATENT APPLICATION

DOCUMENT NAME: PATENT APPLICATION

TO: COMMISSIONER

DATE: February 25, 2003

TITLE OF THE INVENTION: METHOD AND APPARATUS FOR DRIVING PLASMA DISPLAY PANEL

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Nationality: Republic of Korea

The present application is filed pursuant to Article 42 of the Korea Patent Act.

Patent Attorney

Young Ho KIM

[ABSTRACTS]

[ABSTRACT]

The present invention relates to a method of driving a plasma display panel that is adapted for reducing power consumption required for an addressing discharge and decreasing the heat generated in a data driving circuit, and an apparatus for driving a plasma display panel, are disclosed.

The method and the apparatus for driving the plasma display panel select on-cells by applying data of a first voltage and a scan pulse to cells and select off-cells by applying data of a second voltage the scan pulse to cells, wherein the second voltage is higher than the first voltage.

[REPRESENTATIVE DRAWING]

FIG. 7

[SPECIFICATION]

[TITLE OF THE INVENTION]

METHOD AND APPARATUS FOR DRIVING PLASMA DISPLAY PANEL

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 is a schematic plane view of a related art of a plasma display panel;

FIG. 2 is a configuration of a frame for explaining a driving method of the related art plasma display panel;

FIG. 3 is a driving waveform used in the related art plasma display panel;

FIG. 4 is a diagram showing the change of a wall charge on an on-cell when the driving waveform as shown in FIG. 3 is supplied to the related art plasma display panel;

FIG. 5 is a diagram showing the change of a wall charge on an off-cell when the driving waveform as shown in FIG. 3 is supplied to the related art plasma display panel;

FIG. 6 is a block diagram schematically showing an apparatus for driving a plasma display panel according to an embodiment of the present invention;

FIG. 7 is a waveform diagram showing a driving waveform of a plasma display panel according to the embodiment of the present invention;

FIG. 8 is a diagram showing the change of a wall charge

on an on-cell when the driving waveform as shown in FIG. 7 is supplied to the plasma display panel of the present invention; and

FIG. 9 is a diagram showing the change of a wall charge on an off-cell when the driving waveform as shown in FIG. 8 is supplied to the plasma display panel of the present invention.

<DETAILED DESCRIPTION OF THE REFERENCE NUMERALS>

60: Timing controller
61: Data driver
62: Scan driver
63: Sustain driver
64: Driving voltage generator

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[TECHNICAL FIELD INCLUDING THE INVENTION AND PRIOR ART THEREIN]

The present invention relates to a plasma display panel, and more particularly to a method of driving a plasma display panel that is adapted for reducing power consumption required for an addressing discharge and decreasing the heat generated in a data driving circuit, and an apparatus for driving a plasma display panel.

Generally, a plasma display panel radiates a phosphorus using an ultraviolet ray with a wavelength of 147nm generated

upon discharge of an inactive mixture gas, such as He+Xe, Ne+Xe or He+Ne+Xe, to thereby display a picture including characters and graphics. Such a plasma display panel is easy to be made into a thin-film and large-dimension type. Moreover, the plasma display panel provides an improved picture quality with the aid of a recent technical development. Particularly, since the plasma display panel using a three-electrode, alternating current (AC) surface-discharge PDP has properties to reduce voltage needed to the discharge using wall charges accumulated on the dielectric surface thereof upon the discharge and to protect electrodes from a sputtering generated by the discharge with dielectric, it has advantages of a low-voltage driving and a long life.

Referring to FIG. 1, in a related art of the three-electrode, alternating current (AC) surface-discharge PDP, n-number of scan electrodes Y1 to Yn and n-number of common sustain electrodes Z are intersected to m-number of address electrodes X1 to Xm with having a discharges space therebetween wherein m×n-number of cells 1 are located in the intersection. A barrier rib 2 is formed between adjacent address electrodes X1 to Xm in order to intercept electrical and optical interference caused among the horizontally adjacent cells 1.

The scan electrodes Y1 to Yn select scan lines when scan

signals are sequentially applied thereto and occur a sustain discharge for the selected cells when sustain pulses are applied thereto. The common sustain electrodes Z occur the sustain discharge for the cells selected by the sustain pulses and their alternating sustain pulses supplied to the scan electrodes Y1 to Yn. The address electrode X1 to Xm select cells 1 in response to data pulses synchronized with the scan signals.

In order to express gray levels of a picture, the plasma display panel is driven with time division scheme wherein one field period (e.g., NTSC system: 16.67ms) is divided into a plurality of sub-fields having a different light-emission frequency. Each sub-field includes a reset period to initialize cells of full screen, an address period to select a scan line and in turn a cell in the selected scan line, and a sustain period (or a write period) to express gray levels depending upon a discharge frequency. For instance, when it is intended to display a picture with 256 gray levels, a frame period (i.e., 16.67 ms) corresponding to 1/60 second is divided into eight (8) sub-fields SF1 to SF8 as shown in FIG. 2. As described above, each of the 8 sub-fields SF1 to SF8 is divided again into the reset period, the scan period and the sustain period. Herein, the reset period and the address period of each sub-field are identically repeated for every

sub-field, whereas the sustain period is increased at a ratio of 2^n (wherein n = 0, 1, 2, 3, 4, 5, 6 and 7) at each sub-field.

In FIG. 2, reference numerals 'SC1 to SCn' represents n-number of scan lines formed in the PDP.

FIG. 3 shows a driving signal supplied to the PDP for one sub-field period. FIG. 4 and FIG. 5 illustrate the change of a wall charges when the driving signal as in the FIG. 3 is applied to the PDP, respectively.

Referring to FIG. 3 to FIG. 5, the plasma display panel is driven by a reset period for initializing entire cells, an address period for selecting a cell, and a sustain period for sustaining a discharge of the selected cell.

In the reset period, a rising ramp waveform Ramp-up is simultaneously applied to all of the scan electrodes Y. At this time, zero(0) V is applied to a sustain electrodes Z and address electrodes X. The rising ramp waveform Ramp-up cause a set-up discharge of a dark discharge type that the light does not almost generate between the scan electrodes Y and the address electrodes X, and at the same time, cause the set-up discharge of the dark discharge type between the scan electrodes Y and the sustain electrodes Z. By this set-up discharge, positive wall charges are accumulated on the address electrodes X and the sustain electrodes Z, and negative wall charges are accumulated on the scan electrodes Y.

In this connection, the amount of the negative wall charges accumulated on the scan electrodes Y is equal to that of the positive wall charges accumulated on the address electrodes X and the sustain electrodes Z.

Following the rising ramp waveform Ramp-up, a falling ramp waveform Ramp-down falling from a positive voltage lower than a peak voltage of the rising ramp waveform Ramp-up to the ground voltage GND or a specific negative voltage level is simultaneously applied to all of the scan electrodes Y. At the same time, a positive sustain voltage Vs is applied to the sustain electrodes Z, and zero(0) V is applied to the address electrodes X. In this way, when the falling ramp waveform Ramp-down is applied, a set-down discharge of a dark discharge type that the light does nearly generate, is occurred between the scan electrodes Y and the sustain electrodes Z. A discharge is not generated in a section where the falling ramp waveform Ramp-down is falling between the scan electrode Y and the address electrode X, and a dark discharges is generated at a lower limit point. By the set-down discharge, an excessive wall charge that is unnecessary in an address discharge is erased. As a result of the set-down discharge, there is little the change of the wall charges on an address electrode X, whereas the negative walls charge on the scan electrodes Y are decreased and the positive wall charges accumulated on the

sustain electrodes Z are converted into the negative wall charges being accumulated on the sustain electrodes Z by the amount of the decrease of the negative wall charges on a scan electrode Y.

In the address period, zero(0) V or a negative scan pulse SCN of a negative scan voltage -Vy is sequentially applied to the scan electrodes Y and, at the same time, a positive data pulse DATA of a data voltage Vd is applied to the address electrodes X. A voltage difference between the scan pulse SCN and the data pulse DATA is added to the wall voltage generated in the reset period to thereby cause an address discharge, as shown in the FIG. 4 within an on-cell supplied with the data pulse DATA. The wall charges enough to occur the discharge when the sustain voltage Vs is applied are formed within on-cells selected by the address discharge. At this time, the positive wall charges are accumulated on the scan electrodes Y and the negative wall charges are accumulated on the address electrodes X by the address discharge. On the other hand, as shown in the FIG. 5, the address discharge does not occur in an off-cell under the condition that not data voltage Vd but zero(0) V is applied to the address electrode X or that not the scan pulse SCN but a scan bias voltage Vscb is applied to the scan electrodes Y because the sum of a wall voltage created in the reset period and an external voltage is lower

than a firing voltage (which cause to occur discharge between cells). Thus, in the off cell, the wall charges are still maintained in the address and the sustain periods after the reset period.

In the sustain period, after a sustain pulse SUS of the sustain voltage Vs is applied to the scan electrodes Y, the sustain pulse SUS is alternately applied to the sustain electrodes Z and the scan electrodes Y. Consequently, a wall voltage within the on-cells selected by the address discharge is added to the sustain voltage Vs, and whenever each sustain pulse SUS is applied thereto, as shown in the FIG. 4, the sustain discharge, that is, a display discharge occurs between the scan electrodes Y and the sustain electrodes Z in the on-cells. On the other hand, the sustain discharge does not occur in non-selected cells that are not selected in the address period because the sum of the wall voltage within the non-selected cells and an external voltage is lower than the firing voltage, as shown in the FIG. 5.

After the completion of the sustain discharge, an erasing signal (not shown) for erasing the wall charge remaining within the cells is applied to the scan electrodes Y or the sustain electrodes Z.

In this manner, in the related art of the plasma display panel, a high data voltage Vd should be applied to the address

electrodes X in order to select the on-cells in the address period, which leads to flow an excessive current between the address electrodes X and the scan electrodes Y due to the address discharge occuring in the on-cells. Owing to this, the related art plasma display panel has drawbacks that power consumption is increased and the heat generated in data driving integrated circuit IC for driving the address electrodes X becomes higher. As a result, the related art plasma display panel has a problem in that credibility is decreased.

[TECHNICAL SUBJECT MATTER TO BE SOLVED BY THE INVENTION]

Accordingly, it is an object of the present invention to provide a method of driving a plasma display panel and adapted for decreasing power consumption required for an address discharge and reducing the heat generated in a data driving circuit of the plasma display panel, and an apparatus for driving the plasma display panel.

[CONFIGURATION AND OPERATION OF THE INVENTION]

In order to achieve these and other objects of the invention, a method of driving a plasma display panel according to an embodiment of the present invention comprises initializing cells; selecting on-cells by applying data of a

first voltage and scanning pulse to the cells; and selecting off-cells by applying data of a second voltage higher than a first voltage and a scanning pulse to the cells.

The step of initializing the cells includes supplying the same waveform to the scanning electrode and the sustain electrode to form a wall charge having the same polarity at the scanning electrode and the sustain electrode.

The step of supplying the same waveform to the scanning electrode and the sustain electrode simultaneously supplies a rising ramp waveform following a falling ramp waveform to the scanning electrode and the sustain electrode.

The falling ramp waveform falls from a first negative voltage to a second negative voltage having the absolute value higher than that of the first negative voltage.

The rising ramp waveform rises from the first negative voltage to zero(0)V.

A first voltage to select the on-cells is any one of zero(0)V and the ground voltage GND.

The scanning pulse is a positive voltage.

The step of selecting the on-cell includes applying data of the first voltage to an address electrode and, at the same time supplying the positive scanning pulse to the scanning electrode.

The step of selecting the off-cell includes applying data

of the second voltage to the address electrode and, at the same time supplying the positive scanning pulse to the scanning electrode.

The method of driving the plasma display panel further includes applying a sustain pulse to the entire cells to cause a sustain discharge on the on-cells.

An apparatus for driving a plasma display panel according to an embodiment of the present invention comprises a data driver that supplies data of a first voltage and data of a second voltage higher than a first voltage to an address electrode; and a scan driver that initializes cells, and then applies a scanning pulse to a scanning electrode.

A cell to which the data of the first voltage and the scanning pulse is applied is selected as an on-cell, and a cell to which data of the second voltage and the scanning pulse is applied is selected as an off-cell.

The apparatus for driving the plasma display panel further includes a sustain driver that drives a sustain electrode.

The scan driver and the sustain driver supply the same waveform to the scanning electrode and the sustain electrode to form a wall charge having the same polarity at the scanning electrode and the sustain electrode.

The scan driver and the sustain driver simultaneously

supplies a rising ramp waveform following a falling ramp waveform to the scanning electrode and the sustain electrode to initialize the cells.

The scan driver supplies a positive scanning pulse, which is synchronized with data of a first voltage, to the scanning electrode.

The scan driver and the sustain driver alternatively applying a sustain pulse to entire cells to cause a sustain discharge on the on-cells.

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

With reference to FIG. 6 to FIG. 9, there are explained preferred embodiments of the present invention as follows.

Referring to FIG. 6, an apparatus for driving the plasma display panel according to the embodiment of the present invention includes a data driver 61 connected to the address electrodes X1 to Xm of the PDP, a scan driver 62 connected to the scan electrodes Y1 to Yn of the PDP, a sustain driver 63 connected to the sustain electrodes Z of the PDP, a driving voltage generator 64 for supplying driving voltages necessary for the drivers 61, 62, and 63, and a timing controller 60 for controlling each of the drivers 61,62, and 63.

The data driver 61 is supplied with a data that is subjected to an inverse gamma correction and error diffusion by an inverse gamma correction circuit and an error diffusion circuit (not shown) and then mapped by a sub-field mapping circuit to each sub-field. The data driver 61 samples the data in response to a timing control signal CTRX provided from the timing controller 60. The sampled data is supplied to the address electrodes X1 to Xm by one horizontal line for each one horizontal period. Herein, the timing control signal CTRX provided to the data driver 61 includes a sampling clock for sampling the data, and a switching control signal for controlling on/off switching time of an energy recovery circuit and a switching device. A data voltage supplied from the data driver 61 to the address electrodes X1 to Xm is used to a non-selected off-cell.

The scan driver 62 supplies the falling ramp waveform Ramp-down to the scan electrodes Y1 to Yn in the reset period under the control of the timing controller 60 and then supplies the rising ramp waveform Ramp-up to the scan electrodes Y1 to Yn to initialize all cells. Moreover, the scan driver 62 supplies sequentially the positive scan pulse to the scan electrodes Y1 to Yn in the address period under the control of the timing controller 60, and at the same time supplies the sustain pulse to the scan electrodes Y1 to Yn to

cause the cells selected by the address discharge to occur the sustain discharge. A timing control signal CTRY applied to the scan driver 62 includes a switching control signal for controlling on/off switching time of switching devices in the scan driver 62.

The sustain driver 63 supplies, under the control of the timing controller 60, in the reset period, an initializing waveform substantially identical to the initializing waveform that from the scan driver 62, that is, a waveform wherein the falling ramp waveform is continued to the rising ramp waveform, to the sustain electrodes Z. The sustain driver 63 is alternately driven along with the scan driver 62 to supply the sustain pulses to the sustain electrodes Z for the sustain period. A timing control signal CTRZ applied to the sustain driver 63 includes a switching control signal for controlling on/off switching time of switching devices in the sustain driver 63.

The driving voltage generator 64 includes a current-current converter (DC-DC Converter) for converting a system power from a main board (not shown) to a voltage level of output voltage by using a pulse width modulation system. A driving voltage outputted from the driving voltage generator 64 comprises a negative reset voltage -Vrst corresponding to a lower limit voltage of the falling ramp waveform, a negative

voltage -V1 corresponding to a starting voltage of the rising ramp waveform, a positive scan voltage Vsc, a sustain voltage Vs, and a positive data voltage Vd-off for selecting the off-cells.

The timing controller 60 is supplied with a vertical/horizontal synchronization signals, and generates the timing control signals CTRX, CTRY, and CTRZ necessary to drive the drivers 42, 43, and 44, respectively, using the synchronization signals and the main clock.

FIG. 7 shows a driving signal which is supplied to the PDP according to the present invention for one sub-field period. FIG. 8 and FIG. 9 schematically show the change of a wall charge when the driving signal as shown in FIG. 7 is applied to the PDP.

Referring to FIG. 7 to FIG. 9, the plasma display panel according to the embodiment of the present invention is driven in a reset period for initializing all of cells, an address period for selecting a cell and a sustain period for maintaining the discharge of the selected cell.

In the reset period, a falling ramp waveform, Rdn, which is falling from the negative voltage -V1, is simultaneously applied to all of scan electrodes Y1 to Yn and sustain electrodes Z. At the same time, zero(0)V or ground voltage GND is applied to address electrodes X1 to Xm. By the falling

ramp waveform Rdn, a set-up discharge is concurrently occurred in a dark discharge type between the scan electrodes Y1 to Yn and the address electrodes X1 to Xm and, between the sustain electrodes Z and the address electrode X1 to Xm within the cells of the full screen. By the set-up discharge, positive wall charges are accumulated on the scan electrodes Y1 to Yn and the sustain electrodes Z, and negative wall charges are accumulated on the address electrodes X.

Following the falling ramp waveform Rdn, a rising ramp waveform Rup, which is rising from -V1 to zero(0) V or the ground voltage GND, is simultaneously applied to both of the scan electrodes Y1 to Yn and the sustain electrodes Z. At this time, the address electrodes X1 to Xm are maintained at zero(0) V or the ground voltage GND. When the rising ramp waveform Rup is applied as set forth above, the set-down discharge is occurred in the dark discharge type between the scan electrodes Y1 to Yn and the address electrodes X1 to Xm, and between the sustain electrodes Z and the address electrodes X1 to Xm. By the set-down discharge, excessive wall charges unnecessary for the address discharge are eliminated. As the result, the wall charges needed for the address discharge are uniformly remained within all of the cells. The distribution of wall charges accumulated when the reset period is ended is as follows. The negative wall charges are remained

on the address electrodes X, whereas the positive wall charges are uniformly remained on the scan electrodes Y1 to Yn and the sustain electrodes Z.

In the address period, a positive scan pulse SCN of a positive scan voltage Vsc is sequentially applied to the scan electrodes Y1 to Yn and, at the same time, a positive data pulse DATA-OFF of a positive Vd-off or zero(0) V (or the ground voltage GND) is applied to the address electrodes X1 to Xm. External voltage is added to the wall charges accumulated on on-cells and then the address discharge is occurred within the on-cells. By the address discharge, when the sustain voltage Vs is applied, the wall charges enough to occur the discharge are formed on the selected cells, as shown in FIG. 8. At this time, the negative wall charges are accumulated on the scan electrodes Y1 to Yn and the positive wall charge are accumulated on the sustain electrodes Z and the address electrodes X by the address discharge. On the other hand, as shown in the FIG. 9, the address discharge does not occur in an off-cell under the condition that the data voltage Vd-off is applied to the address electrode X1 to Xm and the scan pulse SCN is not applied to the scan electrodes Y because the sum of a wall voltage created in the reset period and an external voltage is lower than the firing voltage. Thus, in the off cell, the wall charges are still maintained in the

address and the sustain periods after the reset period.

In the sustain period, after a sustain pulse SUS of the sustain voltage Vs is applied to the sustain electrodes Z, the sustain pulse SUS is alternately applied to the scan electrodes Y1 to Yn and the sustain electrodes Z. Thus, a wall voltage within the on-cells selected by the address discharge is added to the sustain voltage Vs and, whenever each sustain pulse SUS is applied, as shown in the FIG. 8, the sustain discharge, that is, a display discharge occurs between the scan electrodes Y1 to Yn and the sustain electrodes Z in the on-cells. On the other hand, the sustain discharge does not occur because the sum of the wall voltage within the non-selected cells and an external voltage is lower than the firing voltage, as shown in the FIG. 9.

After the completion of the sustain discharge, an erasing signal (not shown) for erasing the wall charge remaining within the cells is applied to the scan electrodes Y or the sustain electrodes Z.

As a result, the method and the apparatus for driving the plasma display panel according to the present invention occur the address discharge with a low voltage settled as zero(0) V or the ground voltage GND to select the on-cells, and apply a positive scanning voltage to a scanning electrode to select a cell applying a positive voltage as an off-cells where an

address discharges is not generated.

[EFFECT OF THE INVENTION]

As described above, the method and the apparatus for driving the plasma display panel according to the present invention selects the on-cells with a low data voltage such as zero(0) V or ground voltage GND and selects the off-cells which do not occur the address discharge with a high data voltage. As a result, in the method and the apparatus for driving the plasma display panel, power consumption is lowered because voltage applied to the data electrodes in the address discharge is minimized and power consumption is further lowered because the address discharge does not occur in the off-cells to which a relatively high voltage is applied and there is no current generated accordingly. Furthermore, in the method and the apparatus for driving the plasma display panel, it is possible to minimize the heat generated in the data driving integrated circuit and to enhance the driving reliability by lowering the voltage needed to the address discharge and the current generated at the address discharge.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather

that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. A method of driving a plasma display panel, comprising:

initializing cells;

selecting on-cells by applying data of a first voltage and scanning pulse to the cells; and

selecting off-cells by applying data of a second voltage higher than a first voltage and a scanning pulse to the cells.

2. The method of driving the plasma display panel according to claim 1, wherein the step of initializing the cells includes supplying the same waveform to the scanning electrode and the sustain electrode to form a wall charge having the same polarity at the scanning electrode and the sustain electrode.

3. The method of driving the plasma display panel according to claim 2, wherein the step of supplying the same waveform to the scanning electrode and the sustain electrode simultaneously supplies a rising ramp waveform following a falling ramp waveform to the scanning electrode and the sustain electrode.

4. The method of driving the plasma display panel according

to claim 3, wherein the falling ramp waveform falls from a first negative voltage to a second negative voltage having the absolute value higher than that of the first negative voltage, and the rising ramp waveform rises from the first negative voltage to zero(0)V.

5. The method of driving the plasma display panel according to claim 1, wherein a first voltage to select the on-cells is any one of zero(0)V and the ground voltage GND, and the scanning pulse is a positive voltage.

6. The method of driving the plasma display panel according to claim 5, wherein the step of selecting the on-cell includes applying data of the first voltage to an address electrode and, at the same time supplying the positive scanning pulse to the scanning electrode.

7. The method of driving the plasma display panel according to claim 5, wherein the step of selecting the off-cell includes applying data of the second voltage to the address electrode and, at the same time supplying the positive scanning pulse to the scanning electrode.

8. The method of driving the plasma display panel according

to claim 1, further includes applying a sustain pulse to the entire cells to cause a sustain discharge on the on-cells.

9. An apparatus for driving a plasma display panel, including an address electrode, a scanning electrode, a sustain electrode, and cells, which are formed at an intersection of the electrodes, comprising:

a data driver that supplies data of a first voltage and data of a second voltage higher than a first voltage to an address electrode; and

a scan driver that initializes cells, and then applies a scanning pulse to a scanning electrode, and

wherein a cell to which the data of the first voltage and the scanning pulse is applied is selected as an on-cell, and a cell to which data of the second voltage and the scanning pulse is applied is selected as an off-cell.

10. The apparatus for driving the plasma display panel according to claim 9, further includes:

a sustain driver that drives a sustain electrode, and

wherein the scan driver and the sustain driver supply the same waveform to the scanning electrode and the sustain electrode to form a wall charge having the same polarity at the scanning electrode and the sustain electrode.

11. The apparatus for driving the plasma display panel according to claim 10, wherein the scan driver and the sustain driver simultaneously supplies a rising ramp waveform following a falling ramp waveform to the scanning electrode and the sustain electrode to initialize the cells.

12. The apparatus for driving the plasma display panel according to claim 11, wherein the falling ramp waveform falls from a first negative voltage to a second negative voltage having the absolute value higher than that of the first negative voltage, and the rising ramp waveform rises from the first negative voltage to zero(0)V.

13. The apparatus for driving the plasma display panel according to claim 9, wherein a first voltage to select the on-cells is any one of zero(0)V and the ground voltage GND, and the scanning pulse is a positive voltage.

14. The apparatus for driving the plasma display panel according to claim 13, wherein the scan driver supplies a positive scanning pulse, which is synchronized with data of a first voltage, to the scanning electrode.

15. The apparatus for driving the plasma display panel according to claim 10, wherein the scan driver and the sustain driver alternatively applying a sustain pulse to entire cells to cause a sustain discharge on the on-cells.

FIG.1

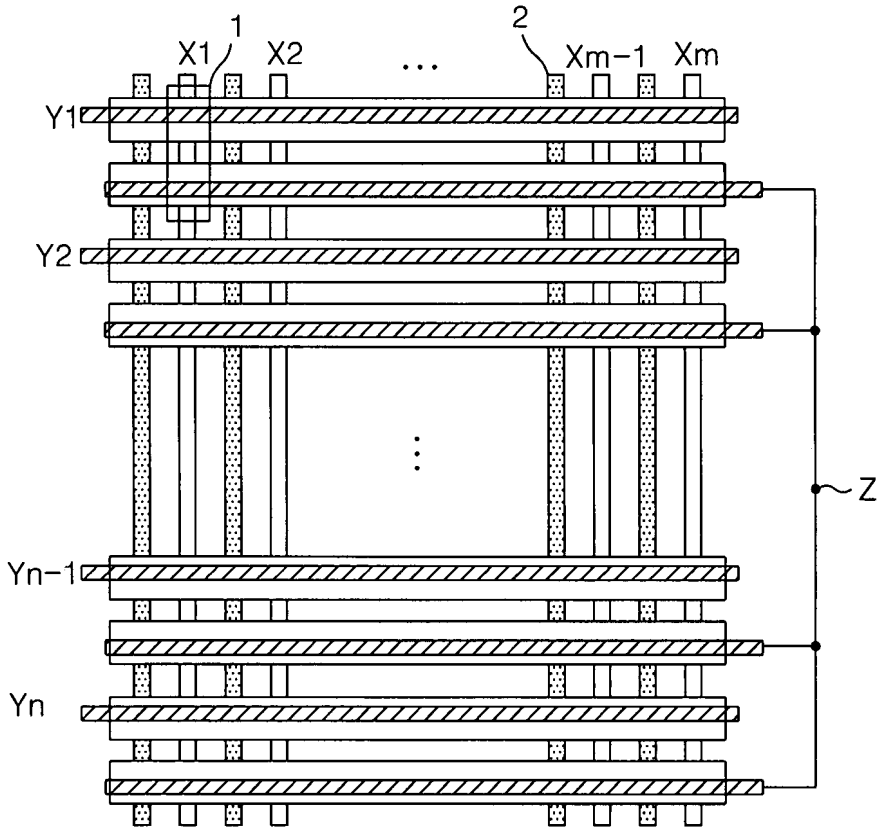


FIG.2

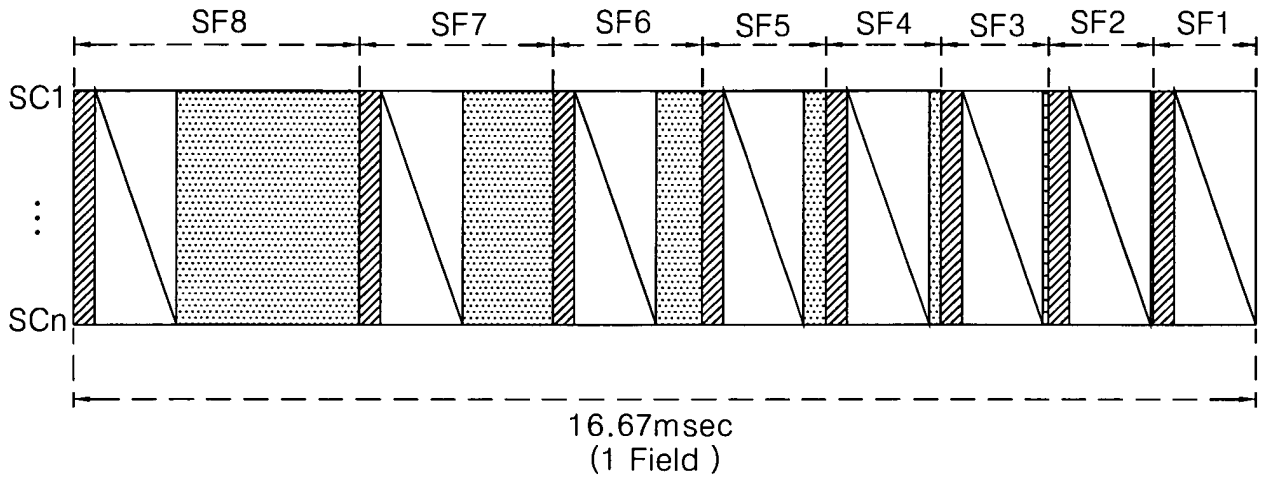
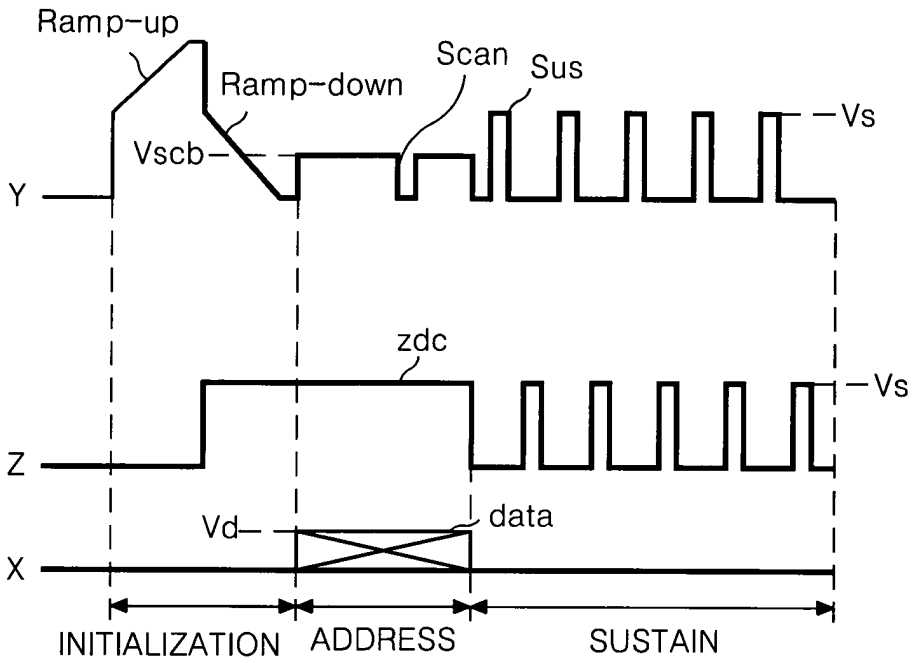

SF8
SF7
SF6
SF5
SF4
SF3
SF2
SF1
SC1
SCn
16.67msec
(1 Field)
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD

FIG.3


Ramp-up
Ramp-down
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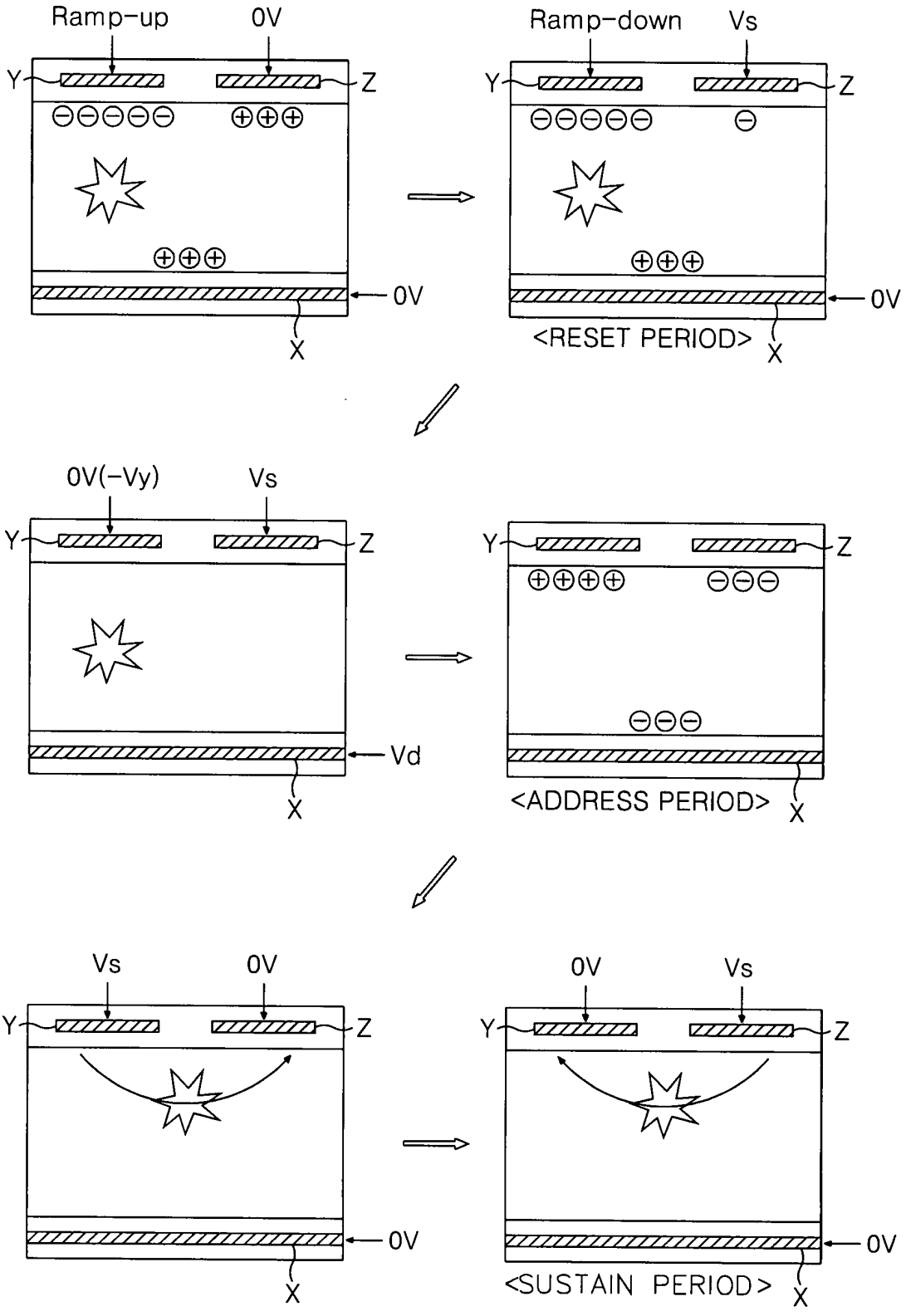
Vscb
Y
zdc
Vs
Z
Vd
data
X
INITIALIZATION
ADDRESS
SUSTAIN

FIG.4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Y
Z
0V
X
Ramp-down
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Y
Z
0V
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0V(-Vy)
Vs
Y
Z
Vd
X
Y
Z
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Vs
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Z
0V
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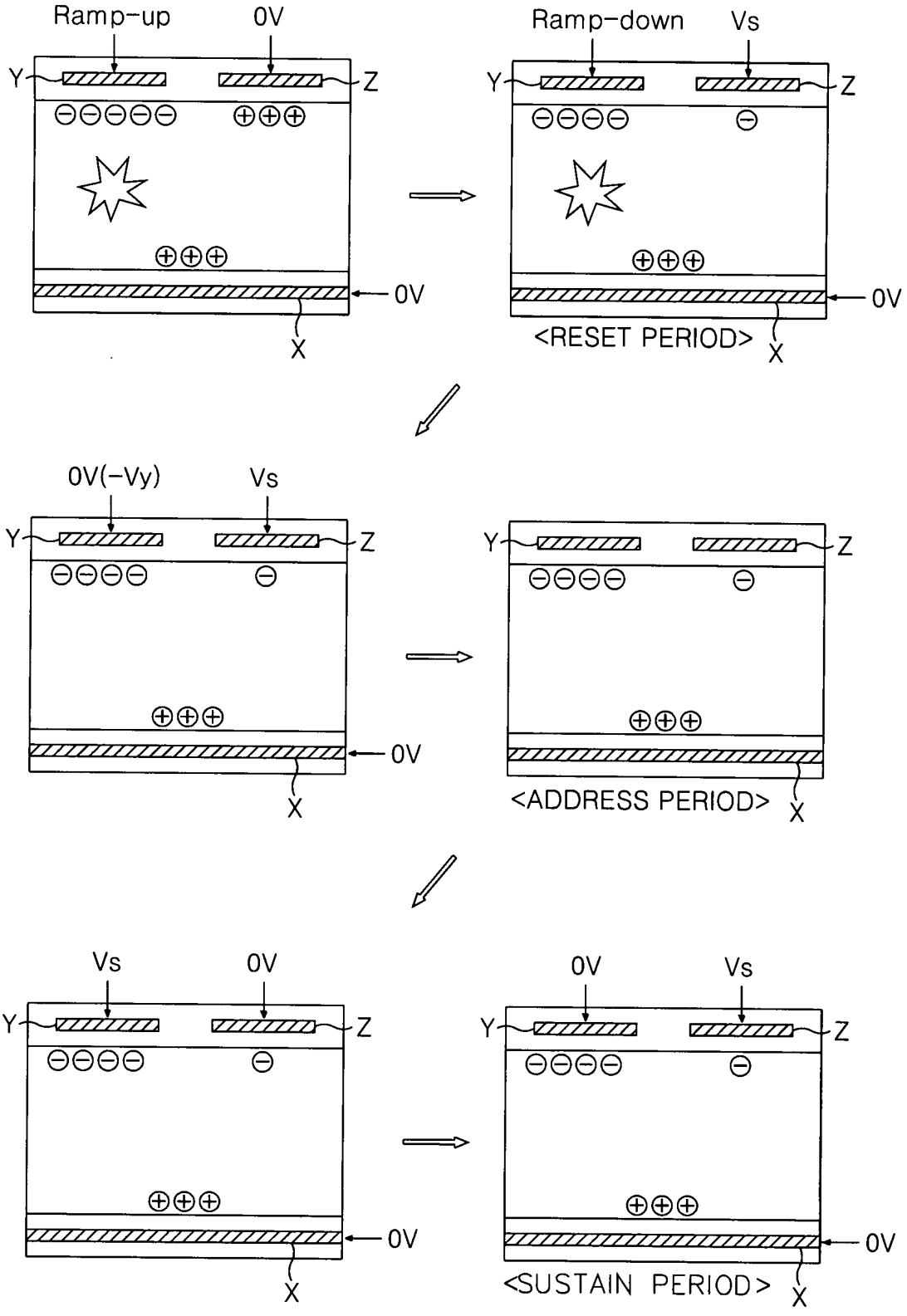
X

FIG.5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Y
Z
0V
X
Ramp-down
Vs
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<SUSTAIN PERIOD>

FIG.6

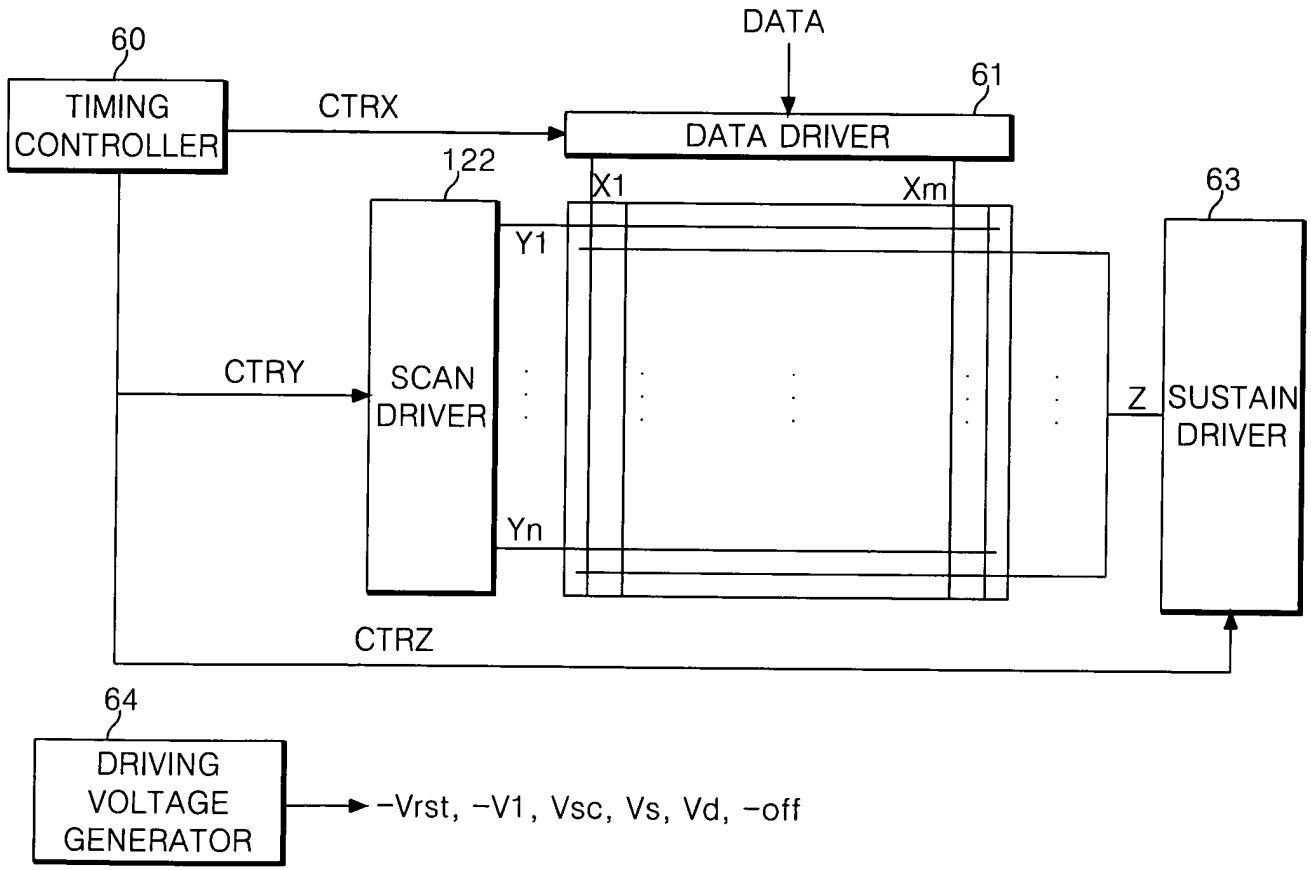

60
TIMING CONTROLLER
CTRX
DATA
61
DATA DRIVER
122
X1
Xm
63
Y1
CTRY
SCAN DRIVER
Z
SUSTAIN DRIVER
Yn
CTRZ
64
DRIVING VOLTAGE GENERATOR
-Vrst, -V1, Vsc, Vs, Vd, -off

FIG.7

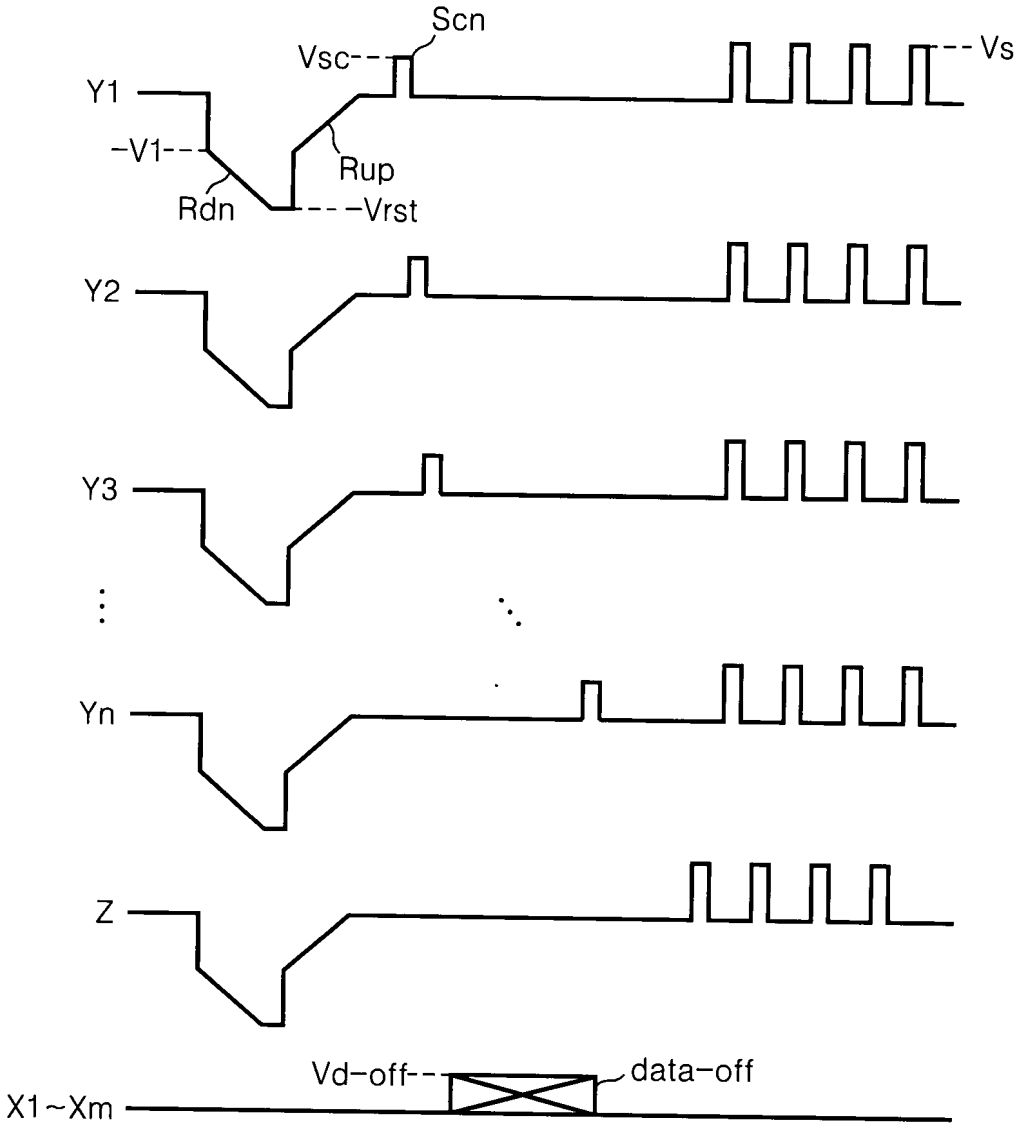


FIG.8

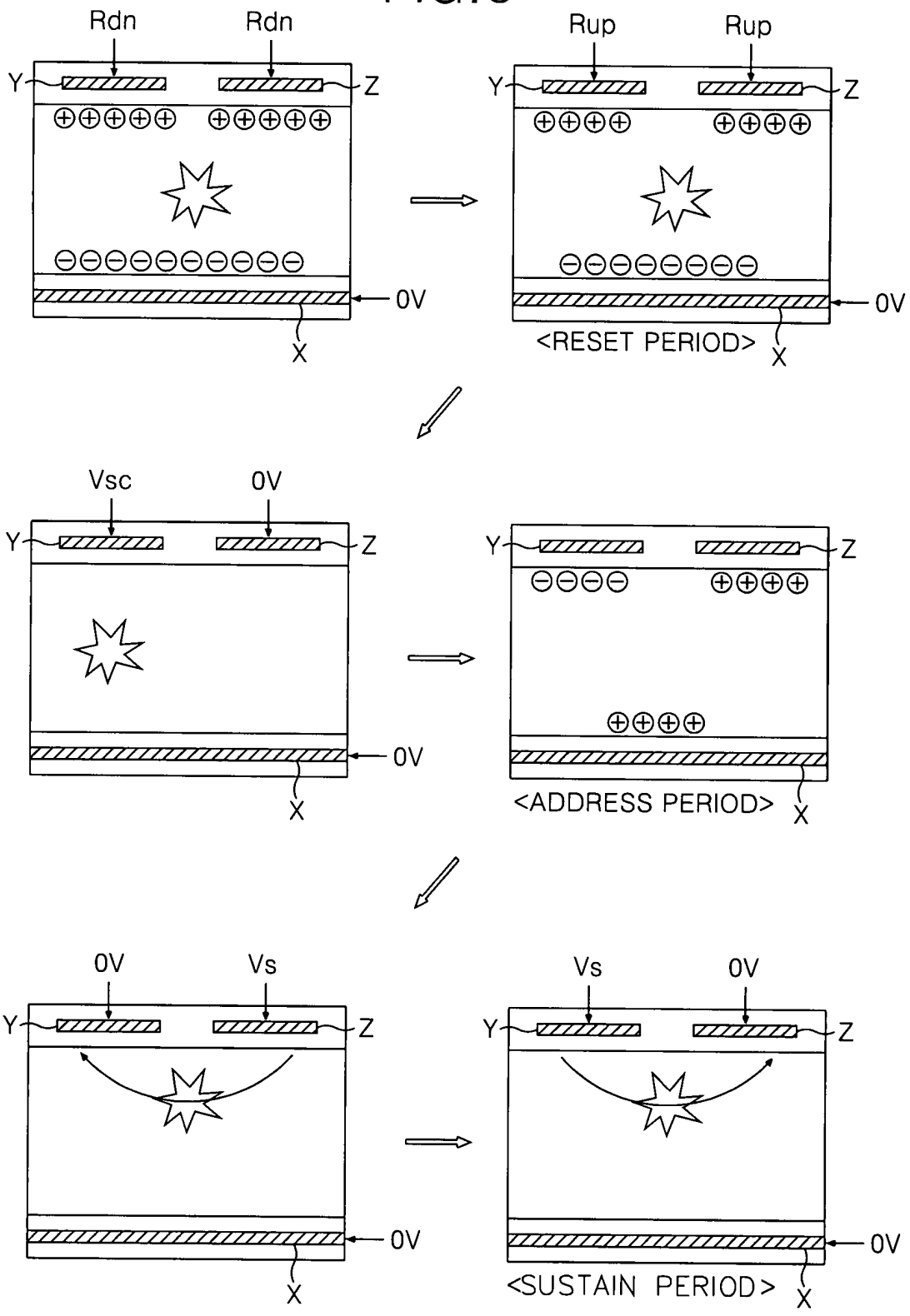
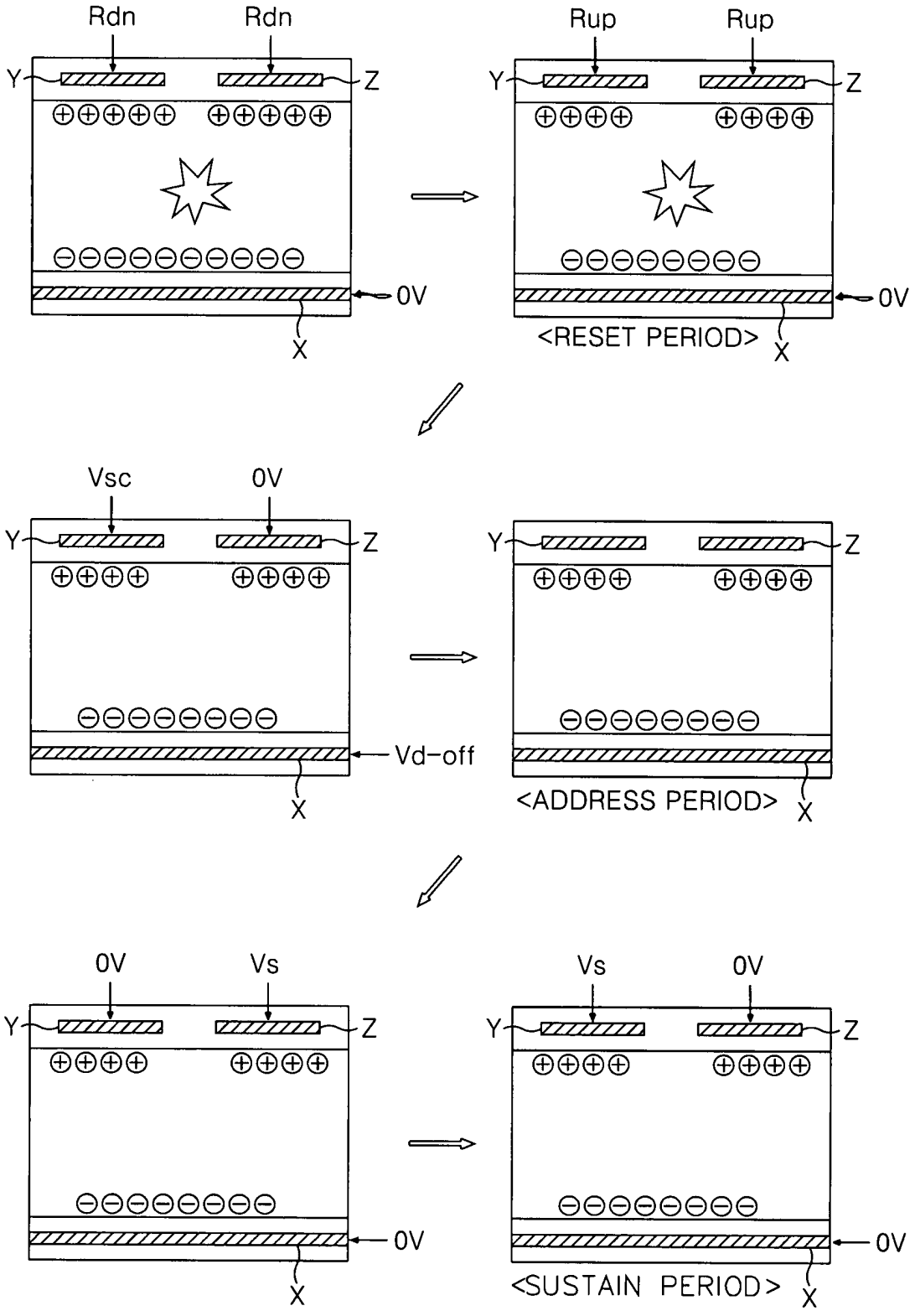

Rdn
Rdn
Y
Z
0V
X
Rup
Rup
<RESET PERIOD>
Vsc
0V
<ADDRESS PERIOD>
0V
Vs
Vs
0V
<SUSTAIN PERIOD>

FIG.9


Rdn
Rdn
Y
Z
0V
X
Rup
Rup
<RESET PERIOD>
Vsc
0V
Vd-off
<ADDRESS PERIOD>
0V
Vs
Vs
0V
<SUSTAIN PERIOD>